REMARKS/ARGUMENTS

Claim Rejections 35 U.S.C. § 102

Claims 1-28 are rejected, under 35 U.S.C. §102(e), as being allegedly anticipated by Nemecek et al., U.S. Pat. No. 7,089,175 (hereinafter, Nemecek). Applicant respectfully traverses the rejection in view of the following.

Independent Claim 1 recites a limitation whereby upon receiving a first signal from an operating program that indicates that a sleep function is to be performed, initiating the sleep function at the device under test, as claimed. Accordingly, the first signal initiating the sleep function is based on an operating system which differs from a hardware source. Independent Claim 1 further recites a limitation whereby one or more clocks of the device under test are turned off, as claimed.

The rejection, in response to Applicant's argument filed on December 18, 2006, asserts that:

"suspending processes can be done in software (in an operating system) or in hardware (by turning off a clock). Nemecek is completely silent about the use of an operating system to activate the sleep mode in the device under test, and instead indicates that the triggers for the sleep and debug modes are hardware signals (see col. 16, lines 42-47 and col. 17, lines 6-15). Examiner therefore finds it inherent that Nemecek places the device in sleep mode by hardware means (turning off a clock)."

Accordingly, independent Claim 1 distinguishes over Nemecek by reciting receiving a first signal from an operating program that indicates that a sleep function is to be performed, as claimed.

Moreover, Nemecek discloses that microcontroller in sleep mode does not interrupt programming operations of the microcontroller in socket 620 (see Nemecek, col. 16, lines 29-31). Nemecek further discloses that the In-Circuit Emulation system pulls the data0 line to a logic low and releases the reset line while holding the data0 line at a logic low to enter the sleep mode (see Nemecek, col. 16, lines 43-47). Nemecek also discloses that this data is clocked into the microcontroller in socket until all of the program lines have been clocked upon which the microcontroller in socket can be removed (see Nemecek, col. 16, lines 63-67). Accordingly, while Nemecek teaches pulling the data line to a logic low, releasing the reset line and holding the data line at a logic low, it fails to explicitly teach turning off one or more clock, as claimed (see Nemecek Figure 8 and accompanying description).

The rejection seems to equate turning off one or more clocks, as claimed to the sleep mode as disclosed by Nemecek by asserting that the definition of sleep is to "suspend operation without terminating" or "temporary state of suspension during which a process remains in memory, so that some event, such as an interrupt or a call from another process, can awaken it." Applicant

respectfully submits that either definition presented by the rejection fails to either teach or suggest turning off one or more clocks, as claimed. For example, suspending operation without terminating may be through receiving signals (e.g., clock signals) but disregarding them which is different than turning off one or more clocks, as claimed. Similarly, a temporary state of suspension may be a breakpoint (e.g., during debugging) upon which clock signals are received, however, no further processing is done until the breakpoint is removed which is also different than turning off one or more clocks, as claimed. Accordingly, either definition presented and interpreted by the rejection fails to teach or suggest turning off one or more clocks, as claimed.

Furthermore, Nemecek discloses that in embodiment of Figure 2, the microcontroller 232 carries out its normal functions needed for debugging the FPGA 220 (see Nemecek, col. 7, lines 13-16). Nemecek further discloses that in embodiment of Figures 8 and 10, the microcontroller 232 is placed in a sleep mode to avoid disrupting programming operations of the microcontroller in socket 620 and that when microcontroller 232 is in debug mode, there is normally no microcontroller present in socket 620 to disrupt the debug operation (see Nemecek, col. 16, lines 29-37). Accordingly, Nemecek teaches the presence of the microcontroller in socket 620 only during programming, thereby disclosing the sleep mode only during programming and not during normal operation of the microcontroller 232.

Accordingly, there is normally no microcontroller present in socket 620 during normal operation of embodiment of Figure 2, thereby no sleep mode is utilized. In contrast, during programming of the microcontroller in socket 620 as disclosed in embodiment of Figures 8 and 10, a sleep mode is utilized. Accordingly, the two cited embodiments are separate embodiments that are incompatible for combination because in one embodiment (e.g., normal function) there is normally no microcontroller in socket 620 and thereby no sleep mode is utilized, whereas in the other embodiment, there is a microcontroller present in socket 620 and thereby a sleep mode is utilized. As such, the two cited embodiments are not combinable.

The rejection relies on the embodiment of Figure 2 to show executing instructions and emulating the functions in lock-step fashion, as claimed. In contrast, the rejection relies on the embodiment of Figures 8 and 10 to show performing a sleep operation, as claimed. However, the two embodiments are not combinable as described above. Applicant respectfully reminds the Examiner that anticipation requires the disclosure in a single prior art reference of each claim under consideration. However, it is not sufficient that the reference recite all the claimed elements. As stated by the Federal Circuit, the prior art reference must disclose each element of the claimed invention "arranged as in the claims" (see Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730

F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)). Accordingly, choosing elements from different embodiments (e.g., Figure 2 and Figures 8 and 10 of Nemecek) fails to teach the recited limitations in the arranged claimed fashion because the two relied upon embodiments are not combinable.

Accordingly, Nemecek fails to anticipate independent Claim 1, under 35 U.S.C. §102(e). Independent Claims 10 and 25 recite limitations similar to that of independent Claim 1 and are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency.

As per, Claims 4, 13 and 26, the rejection interprets that a "key code" disclosed by Nemecek corresponds to the claimed number of clock signals received ... that equals a predetermined value, as claimed. Applicant respectfully disagrees. Nemecek discloses that a key code is clocked in order to prevent unauthorized modification of the program and if the key code does not match the microcontroller then the socket begins running whatever code is stored internally (see Nemecek, col. 16, lines 51-56). Accordingly, the key code is a method of authenticating a user (e.g., encryption, password and etc.). The Applicant does not understand authenticating the user to either teach or suggest determining the number of clock signals received, as claimed. Moreover, Nemecek discloses that when programming is done, the ICE system turns off power such that the programmed microcontroller can be removed (see Nemecek, col. 16, lines 63-67

and Figure 10 element 856). In contrast, Nemecek teaches away by disclosing turning off the power instead of resuming execution, as claimed. As such, Nemecek fails to teach resuming execution when the determined number of clock signals received at the emulator device equals a predetermined value, as claimed.

Independent Claim 7 recites a limitation whereby upon receiving the first signal, discontinuing the sending of the clock signals from the device under test to the emulator device, as claimed.

The rejection in response to Applicant's argument filed on December 18, 2006 asserts that Nemecek "expressly teaches in lines 1-10 of col. 16 that once the microcontroller 232 is in sleep mode, it does not disturb the programming process" and that "Nemecek teaches in lines 30-34 of col. 16 that FIG. 10 depicts a process 800 used to place the microcontroller 232 in a sleep mode so that it does not disrupt programming operations of the microcontroller in socket 620." However, the rejection relies on the embodiment of Figure 2, as disclosed in Nemecek, to show the remainder of the recited limitations. As discussed above with respect to Claim 1, choosing elements from different embodiments (e.g., Figure 2 and Figures 8 and 10 of Nemecek) fails to teach the recited limitations in the arranged claimed fashion because the two relied upon embodiments are not combinable.

Moreover, Nemecek discloses that the ICE asserts U_D0-BRQ (break) to stop the microcontroller and after halting it may issue commands to query the status of various registers and memory locations of the virtual microcontroller (see Nemecek, col. 13, lines 6-15). The Applicant does not understand stopping the microcontroller from further processing to necessarily equate to or suggest discontinuing the sending of the clock signals, as claimed. Similarly, Nemecek discloses that when an interrupt request is pending for the microcontroller, the system asserts U_D1_IRQ as an interrupt request (see Nemecek, col. 13, lines 16-20). Applicant does not understand a pending interrupt to either teach or suggest discontinuing the sending of the clock signals, as claimed.

Furthermore, Nemecek discloses that when the microcontroller undergoes a watchdog reset, it asserts IRQ (interrupt) and BRQ (break) lines indefinitely that stops the microcontroller clock (see Nemecek, col. 13, lines 46-50). Applicant does not understand stopping the microcontroller clock to equate to discontinuing the sending of the clock signals, as claimed because a clock may be on and yet clock signals not sent whereas Nemecek discloses necessarily stopping the microcontroller's clock.

Accordingly, Nemecek neither teaches nor suggests the limitations of independent Claim 7 and is patentable, under 35 U.S.C. §102(e). Independent

Claims 16 and 21 recite limitations similar to that of independent Claim 7 and are patentable over Nemecek for similar reasons. Dependent claims are patentable by virtue of their dependency.

As such, allowance of Claims 1-28 is earnestly solicited.

For the above reasons, the Applicant requests reconsideration and withdrawal of rejections under 35 U.S.C. 102(e).

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-28 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-28 overcome the rejections of record and, therefore, allowance of Claims 1-28 is earnestly solicited.

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Respectfully submitted,
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